Claims

[c1] 1. A layout structure for supporting two different package techniques of the central processing units (CPUs) , wherein said layout structure is placed in an area where is between a control chip and said CPU , said layout structure comprising:
a top signal layer, used to place a first signal line in said area where said CPU is coupled to the control chip;
a reference potential providing layer, located below said top signal layer, coupled to a reference potential, wherein said first signal line refers to the reference potential providing layer;
a power layer, located below said reference potential providing layer, comprising:
a voltage providing area for providing an operating voltage to the CPU and said control chip; and
a reference potential providing area, coupled to the reference potential; and
a bottom signal layer, located below said power layer, used to place a second signal line in said area where said CPU is coupled to the control chip, wherein said second signal line refers to the reference potential providing area in said power layer.

[c2] 2. The layout structure of claim 1, wherein said reference potential is a grounded potential.

[c3] 3. The layout structure of claim 1, wherein said reference potential providing area is located in a first side of said control chip, and said CPU operating voltage providing area cuts into a second side of said control chip.

[c4] 4. The layout structure of claim 3, wherein said first side is said side nearest to the CPU, and said second side is a contiguous side of said first side.

[c5] 5. The layout structure of claim 1, wherein said CPU is either a CPU that has 423 pins and uses said pin grid array (PGA) package, or a CPU that has 478 pins and uses said ball grid array (BGA) package.

[c6] 6. The layout structure of claim 5, wherein said CPU having 423 pins and said

CPU having 478 pins use a single control chip to support said CPU operation.

[c7] 7. The layout structure of claim 1, wherein said layout structure is placed in a motherboard.

[c8] 8. A motherboard for supporting a plurality of CPUs of two different package techniques, comprising:
a first area, used to place said CPU;
a second area, located in between said CPU and a control chip, comprising:
a top signal layer, used to place a first signal line in said area where said CPU is coupled to the control chip;
a reference potential providing layer, located below said top signal layer, coupled to a reference potential, wherein said first signal line refers to the reference potential providing layer;
a power layer, located below said reference potential providing layer, comprising:
a voltage providing area for providing an operating voltage to the CPU and said control chip; and
a reference potential providing area, coupled to the reference potential; and
a bottom signal layer, located below said power layer, used to place a second signal line in said area where said CPU is coupled to the control chip, wherein said second signal line refers to the reference potential providing area in said power layer.

[c9] 9. The motherboard of claim 8, wherein said reference potential is a grounded potential.

[c10] 10. The motherboard of claim 8, wherein said reference potential providing area is located in a first side of said control chip, and said CPU operating voltage providing area cuts into a second side of said control chip.

[c11] 11. The motherboard of claim 10, wherein said first side is said side nearest to the CPU, and said second side is a contiguous side of said first side.

[c12] 12. The motherboard of claim 8, wherein said CPU is either a CPU that has 423 pins and uses said pin grid array (PGA) package, or a CPU that has 478 pins and

uses said ball grid array (BGA) package.

[c13] 13. The motherboard of claim 12, wherein said CPU having 423 pins and said CPU having 478 pins use a single control chip to support said CPU operation.

[c14] 14. The motherboard of claim 8, further comprising a third area, used to couple to the other element besides said CPU, wherein said third area comprises:
a top signal layer, used to place a third signal line in said area where said other element is coupled to the control chip;
a reference potential providing layer, located below said top signal layer, coupled to a reference potential, wherein said third signal line refers to the reference potential providing layer;
a power layer, located below said reference potential providing layer, comprising a plurality of power cut areas, used to provide an operating voltage for said other element; and
a bottom solder layer, located below said power layer, used to place a fourth signal line in said area where said other element is coupled to the control chip.

[c15] 15. A layout structure for supporting a plurality of central processing units (CPUs) of two different package techniques, placed and coupledwith a first area, wherein said first area is said area where a plurality of signals of a CPU is coupled to a plurality of signals of a control chip, said structurecomprising:
a first signal layer;
a first reference layer, having a first reference potential, wherein a first signal line that is placed on said first signal layer refers to the first reference layer;
a second reference layer, comprising:
a first reference area, having said first reference potential; and
a second reference area, having a second reference potential, used to provide an operating voltage that is needed for said CPU; and
a second signal layer, wherein a second signal line that is placed on said second signal layer refers to the first reference area of said second reference area.

[c16] 16. The layout structure of claim 15, wherein said first reference layer is a grounded layer, said first reference potential is a grounded potential, said second reference layer is a power layer.

[c17] 17. The layout structure of claim 15, wherein all said plurality of signals of said CPU that are coupled to the control chip can be placed on said first signal layer and said second signal layer.

[c18] 18. The layout structure of claim 15, wherein all said plurality of signals of said CPU that are coupled to the control chip refer to the first reference potential.

[c19] 19. The layout structure of claim 15, wherein said CPU having 423 pins and said CPU having 478 pins use a single control chip to support said CPU operation.

[c20] 20. The layout structure of claim 19, wherein said layout structure is placed in a motherboard.

[c21] 21. A motherboard for supporting a plurality of CPUs of two different package techniques, placedbetween a CPU and a control chip, comprising:
a first area, wherein said whole CPU is placed in said range of said first area, said stack structure of said first area along a first direction sequentially comprising:
a first signal layer;
a first reference layer, having a first reference potential;
a second reference layer, comprising:
a first reference area, having said first reference potential; and
a second reference area, having a second reference potential; and
a second signal layer;
a second area, all said plurality of signals of said control chip that are coupled to the CPU are placed in said range of said second area, said stack structure of said second area along said first direction sequentially comprising:
a third signal layer;
a third reference layer, having said first reference potential;
a fourth reference layer, comprising:
a third reference area, having said first reference potential; and
a fourth reference area, having said second reference potential; and
a fourth signal layer; and
a third area, all said plurality of signals of said control chip that are not coupled to the CPU are placed in said range of said third area, said stack structure of

said third area along said first direction sequentially comprising:
a fifth signal layer;
a fifth reference layer, having said first reference potential;
a sixth reference layer, having a plurality of reference areas that have a plurality of other reference potentials; and
a sixth signal layer.

[c22] 22. The motherboard of claim 21, wherein said first reference layer, said third reference layer, and said fifth reference layer are a grounded layer, said first reference potential is a grounded potential; said second reference layer, said fourth reference layer, and said sixth reference layer are a power layer, said second reference potential is a core potential, other reference potentials are said power potential needed by said control chip besides said grounded potential and said core potential.

[c23] 23. The motherboard of claim 21, wherein all said plurality of signals of said CPU on said printed circuit board that are coupled to the control chip can be placed on said first signal layer, said second signal layer, said third signal layer and said fourth signal layer, said plurality of signals that are placed on said second signal layer and said fourth signal layer refer to the first reference area and said third reference area respectively.

[c24] 24. The motherboard of claim 21, wherein all said plurality of signals of said CPU on said printed circuit board that are coupled to the control chip refer to the first reference potential.

[c25] 25. The motherboard of claim 21, wherein said third reference area of said fourth reference layer is located in a first side of said control chip, said fourth reference area of said fourth reference layer cuts into a second side of said control chip.

[c26] 26. The motherboard of claim 25, wherein said first side is said side nearest to the CPU, and said second side is a contiguous side of said first side.

[c27] 27. The motherboard of claim 21, wherein said CPU is either a CPU that has 423 pins and uses said pin grid array (PGA) package, or a CPU that has 478 pins and

uses said ball grid array (BGA) package.

[c28] 28. The motherboard of claim 21, wherein said CPU having 423 pins and said CPU having 478 pins use a single control chip to support said CPU operation.

[c29] 29. A layout method for supporting a plurality of CPUs of different package techniques, comprising:
providing a plurality of printed circuit boards;
placing on said printed circuit board that is used to constitute a top signal layer and a bottom signal layer, wherein said placement can be processed on said top signal layer and said bottom signal layer in said area where said control chip is coupled to the CPU;
cutting said printed circuit board that is used to constitute a power layer to cut off an area that is coupled to a reference potential on said power layer in said area where said control chip is coupled to the CPU; and
combining said printed circuit board to form a stack structure.

[c30] 30. The layout method of claim 29, wherein said stack structure comprises:
said top signal layer, used to place a first signal line in said area where said CPU is coupled to the control chip;
a reference potential providing layer, located below said top signal layer, coupled to the reference potential;
a power layer, located below said reference potential providing layer, comprising:
a voltage providing area for providing an operating voltage to the CPU and said control chip; and
a reference potential providing area, coupled to the reference potential; and
said bottom signal layer, located below said power layer, used to place a second signal line in said area where said CPU is coupled to the control chip.

[c31] 31. The layout method of claim 29, wherein said first signal line refers to the reference potential providing layer.

[c32] 32. The layout method of claim 29, wherein said second signal line refers to the reference potential providing area of said power layer.

[c33] 33. The layout method of claim 29, wherein said stack structure is located in said area where said plurality of signals of said CPU is coupled to the plurality of signals of said control chip.

[c34] 34. The layout method of claim 33, wherein said layout structure is placed on said motherboard.

[c35] 35. The layout method of claim 29, wherein said reference potential is a grounded potential.

[c36] 36. The layout method of claim 29, wherein said reference potential providing area is located in a first side of said control chip, and said CPU operating voltage providing area cuts into a second side of said control chip.

[c37] 37. The layout method of claim 36, wherein said first side is said side nearest to the CPU, and said second side is a contiguous side of said first side.

[c38] 38. The layout method of claim 29, wherein said CPU is either a CPU that has 423 pins and uses said pin grid array (PGA) package, or a CPU that has 478 pins and uses said ball grid array (BGA) package.

[c39] 39. The layout method of claim 38, wherein said CPU having 423 pins and said CPU having 478 pins use a single control chip to support said CPU operation.